

## CONCATENATED EQUALIZER/TRELLIS DECODER ARCHITECTURE FOR AN HDTV RECEIVER

The present patent application claims priority from provisional patent application no. 60/373,008 filed on April 16, 2002.

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### BACKGROUND

#### 1. Field of the Invention

This invention relates generally to the field of digital signal processing and more particularly to a concatenated equalizer/trellis decoder suitable for decoding multiple mode trellis encoded High Definition Television (HDTV) signals.

#### 2. Background of the Invention

The Advanced Television Systems Committee (ATSC) standard for HDTV in the United States specifies an eight (eight levels per symbol) vestigial sideband (VSB) transmission system as described in the "ATSC Digital Television Standard", Document A/53 published on September 16, 1995. This document sets forth all the requirements regarding HDTV signal characteristics. In the receiver, an equalizer is included which is an adaptive filter which receives the VSB data stream at an average rate equal to the symbol rate of approximately 10.76 MHz. The equalizer attempts to remove linear distortions mainly caused by multipath signal propagation, which is characteristic of terrestrial broadcast channels. One equalizer design suitable for use in an HDTV receiver is a decision feedback equalizer (DFE) as described in John G. Proakis, "Digital Communications", McGraw-Hill, 2nd edition, 1989, New York and in U.S. Patent no. 6,493,409, entitled PHASE DETECTORS IN CARRIER RECOVERY FOR OFFSET QAM AND VSB, issued on December 10, 2002 to Lin et al. A simplified block diagram of a typical DFE architecture is shown in Figure 1. The DFE is seen to include a Feed Forward Filter (FFF), a Feedback Filter (FBF), a slicer, a lock detector

and a mode switch, and is capable of operating in training, blind or decision directed (dd) modes.

The functions of the FFF, FBF and the slicer are well known and together they perform the basic functions of filtering and quantization. The lock detector compares the equalizer output and the slicer levels with a threshold, and in response to that operation generates an updated lock detector output. The mode switch chooses the appropriate input to the FBF filter as well as selecting the error and control signals to be used in performing the equalizer adaptation according to the current equalizer operating mode.

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- 10     The mode switch also examines the lock detector output. In normal operation, the equalizer mode switch has an automatic switching capability, which depends on the status of the equalizer lock detector. The mode switch assumes that the training and blind modes are used for convergence purposes only. After the equalizer lock detector senses convergence, the
- 15     equalizer is then switched to the decision directed (dd) mode. Whenever convergence is lost, the mode switch returns the equalizer to the training or blind mode.

- In the ATSC standard, a training sequence is included in the field sync signal in order to provide a mechanism for initial equalizer convergence. The received sequence of coded symbols serves as the input to a synchronization control unit, which detects field and segment synchronization patterns within the symbol sequence and generates the corresponding sync signals. In the training mode, the equalizer coefficients are only updated during the field sync pulse. The drawbacks of this method are that it requires the prior correct detection of the field sync, and since the training sequence is contained in the field sync, which occurs only once every 25 milliseconds, the rate of convergence is possibly decreased. In an environment of multiple reflected or ghost signals, or in other dynamic environments, the detection of the field sync may be difficult. In those situations the receiver needs some self recovering or blind method of initially adjusting equalizer tap coefficients

without referring to the training sequence. Since a blind algorithm works with every data symbol it will also tend to have a faster rate of convergence. An example of a blind convergence algorithm is Godard's Constant Modulus Algorithm (CMA). See D. N. Godard, "Self-Recovering Equalization and

- 5 Carrier Tracking in Two Dimensional Data Communication Systems", IEEE Transactions on Communications, Vol. COM-28, pp.1867-1875, November 1980. See also D. N. Godard, US Patent 4,309,770.

The final mode of equalizer operation, decision directed (dd), assumes that the input to the feedback filter (FBF) is the output of the slicer. Since the 10 adaptation error and the input to the feedback filter are aided by the presence of the slicer, coefficient adaptation occurs throughout the data sequence. The dd mode does not have good convergence characteristics, but once convergence is achieved it has advantages when compared to the other modes of equalizer operation. The presence of the slicer data results in a 15 reduced mean squared error (MSE) and bit error rate (BER) at the equalizer output when compared to operation in the blind mode. Since the dd mode updates its coefficients with every symbol rather than interpreting just the training symbols, the dd mode provides faster adaptation and tracking capabilities than the training mode.

- 20 Trellis coding is used in combination with other techniques to protect against interference from particular noise sources. Trellis coding requirements for HDTV are presented in sections 4.2.4 – 4.2.6 (Annex D), 10.2.3.9, 10.2.3.10 and other sections of the Digital Television Standards for HDTV Transmission of April 12, 1995 prepared by the ATSC. The HDTV 25 standard presents a trellis coding system that employs an interleaving function involving twelve parallel trellis encoders at a transmitter and twelve parallel trellis decoders at a receiver for processing twelve interleaved data streams. The trellis system employed utilizes a rate 2/3 trellis coded modulation (TCM) code. The code is implemented by coding one bit using a 30 rate ½, four state convolutional encoder, and then adding an FEC uncoded bit

which is differentially precoded. Each set of three coded bits produced by the encoder is mapped to an eight level VSB modulator symbol. Figure 2 is a block diagram showing the differential precoder, trellis encoder and corresponding eight level VSB symbol mapper. The twelve identical encoders  
5 and precoders are used sequentially, processing each one byte at a time and subsequently transmitting one complete symbol at a time. For each encoder, the input data bits X1 and X2 are encoded as three bits Z2, Z1, and Z0. Each three-bit word corresponds to one of the eight symbols R. The input bit X2 is processed by a precoder to provide encoded bit Z2. The input bit X1 is  
10 encoded as two bits Z1 and Z0 by the trellis encoder. An example of a trellis decoder used in an HDTV receiver is disclosed in U.S. Patent no. 5,841,478, entitled CODE SEQUENCE DETECTION IN A TRELLIS DECODER, issued on November 24, 1998 to Hu, et al.

The use of DFE techniques has been the subject of controversy in the  
15 field of receiver design. While DFE offers a relatively simple method for equalizing a highly dispersive linear channel, it may suffer from error propagation, a mechanism whereby incorrect source symbol estimates may cause future decision errors leading to potentially lengthy error bursts. In the HDTV receiver, when the terrestrial channel introduces multipath and white  
20 noise, particularly when the multipath signal is strong and the signal to noise ratio (SNR) is low, error propagation in the feedback filter (FBF) of the equalizer (DFE) affects the performance at the output of the trellis decoder. Simulation of an ATSC receiver including a Decision Feedback Equalizer (DFE) for an HDTV terrestrial channel having strong multipath and Additive  
25 White Gaussian Noise (AWGN) shows that receiver performance can be improved if the decision directed mode is replaced by a soft decision directed mode, whereby the input to the FBF filter is the equalizer output instead of the slicer output. In addition, ideally the equalizer feedback filter should receive more accurate symbol decisions than those provided by the equalizer slicer.

SUMMARY OF THE INVENTION

The present invention provides a further improvement in HDTV receiver performance by using a concatenated equalizer/trellis decoder structure. Re-encoded trellis decoder outputs, rather than the equalizer output, are used as the input signal to the feedback filter of the Decision Feedback Equalizer (DFE). Due to the latency associated with trellis decoding and the fact that the trellis decoder is actually composed of twelve interleaved decoders, the feedback from the trellis decoder to the equalizer cannot be implemented in real time. The present architecture performs the feedback operation by providing an additional trellis decoder and equalizer along with an additional delay unit to provide data synchronization. The structure is modular and each module can be cascaded in as many stages as needed in order to achieve the desired balance between complexity and performance. In addition, a soft output trellis decoding algorithm may be employed to improve performance. Although this disclosure is directed to the ATSC HDTV system, the present invention may also be utilized in any receiver in which a DFE is followed by a trellis or convolutional decoder.

BRIEF DESCRIPTION OF THE DRAWING

Figure 1 is a simplified block diagram of a prior art Decision Feedback  
20 Equalizer architecture;

Figure 2 is a block diagram of an ATSC HDTV trellis encoder,  
differential precoder and symbol mapper;

Figure 3 is a simplified block diagram of the concatenated  
equalizer/trellis decoder system constructed according to the principles of the  
25 present invention;

Figure 4 is a graph showing the bit error rate versus the signal to noise  
ratio at the trellis decoder output for a first set of operating conditions,  
including those achieved by operation of the present invention; and

Figure 5 is a graph showing the bit error rate versus the signal to noise ratio at the trellis decoder output for a second set of operating conditions, including those achieved by operation of the present invention.

#### DETAILED DESCRIPTION

5 Referring to Figure 3, a simplified block diagram of the present invention shows a decision feedback equalizer module 1 that is interconnected to a first equalizer 2 and a trellis decoder 3 as would be present in a conventional DFE. The improved DFE module 1 can be replicated as many times as needed in an HDTV receiver in order to achieve  
10 the desired performance for a given investment in hardware. The DFE module 1 includes a trellis decoder and re-encoder 5, which generates as an output 6 the optimum encoded sequence rather than the optimum decoded sequence. In a conventional ATSC HDTV system, the input data bits X1 and X2 are encoded as three bits Z2, Z1, and Z0, as shown in Figure 2. Each  
15 three-bit word corresponds to one of the eight symbols R. The input bit X2 is processed by a precoder to provide encoded bit Z2. The input bit X1 is encoded as two bits Z1 and Z0 by the trellis encoder. In the DFE module 1, the decoder/re-encoder 5 is able to reduce the need for control and mapping logic which is associated with the bits per branch of a trellis network. Instead,  
20 additional memory is allocated to the decoder/re-encoder 5 for storing the encoded three bits per branch (Z2, Z1, and Z0) instead of the decoded two bits (the input data bits X1 and X2) sequence. The delay unit 7 causes a delay that is equivalent to and thereby accounts for the delay introduced by the decoder/re-encoder 5. The DFE module 1 includes a second equalizer 4  
25 which is similar to the first equalizer 2 except that no slicer is required. Not shown in Figure 3 are the functions of the lock detector and mode switch depicted in Figure 1, which are still required but are not illustrated for the purpose of clarity.

30 The DFE module 1 can be constructed in at least two different forms according to the type of trellis decoder/re-encoder 5 that is utilized. In a first

embodiment, the decoder/re-encoder 5 creates as an output 6 the hard decision data that would be generated by a typical re-encoder unit. This embodiment would create an output 6 that is equivalent to the slicer output in the traditional DFE architecture depicted in Figure 1. However, this output has

5 the advantage of the correction capability provided by the trellis decoder.

In a second embodiment, the output 6 is a soft decision version of the data and is obtained by utilizing a trellis decoder soft output algorithm, such as the soft output Viterbi algorithm (SOVA). See J. Hagenauer and P.

Hoeher, "A Viterbi Algorithm with Soft-Decision Outputs and its Applications",

- 10 Proceedings of GLOBECOM'89, pp.1680-1686, November 27-30/1989, Dallas, TX. Also see U.S. Patent no. 5,467,132, entitled METHOD FOR DIGITAL TRANSMISSION OF HIERARCHICAL HDTV, EDTV AND SDTV TELEVISION SIGNALS, issued on November 14, 1995 to Fazer et al. The SOVA algorithm is a relatively complex trellis decoding algorithm which
- 15 creates a soft output version of the data by defining reliability bits that are a function of the metric values at the decoding instant. Although more complex than the hard decision decoding scheme, the soft output trellis decoder generates an input to the FBF filter 8 that improves immunity to error propagation.

- 20 Let  $L$  be the number of memory elements in the trellis encoder,  $S = 2^L$  be the number of states in the trellis diagram,  $M$  be the channel symbol alphabet size and  $K$  be the number of trellis branches merging to a state. In the ATSC HDTV case,  $(L, S, M, K) = (2, 4, 8, 4)$ . Let  $\underline{I}$  be the transmitted channel symbol vector and  $\underline{Z} = \underline{I} + \underline{N}$  be the received vector where  $\underline{N}$  is an AWGN vector. Assume that the classical Viterbi algorithm (VA) makes a final decision with delay  $\delta$ ,  $\delta$  being large enough so that all  $K$  survivor paths have been merged with sufficiently high probability. The decision consists of selecting the path with the smallest path metric. The path metric for the AWGN channel is given by

$$\Lambda^{(k)} = \frac{E_s}{N_o} \sum_{j=n-\delta}^n (z_j - I_j^{(k)})^2, \quad k = 1, 2, \dots, K \quad (1)$$

where  $n$  is the length of the path,  $I_j^{(k)}$  is the channel symbol for the  $k^{\text{th}}$  path at time  $j$  and  $E_s/N_o$  is the signal-to-noise ratio. With this form, we have

$$P(\underline{Z} | \underline{I}^k) \approx e^{-\Lambda^{(k)}}, \quad k = 1, 2, \dots, K \quad (2)$$

- 5 where  $\underline{I}^{(k)}$  is the channel symbol vector associated with the  $k^{\text{th}}$  path and  $P(\underline{Z} | \underline{I}^k)$  is the conditional probability of the received vector with respect to the channel symbol vector.

The reliability of each path with respect to the received vector is given by

$$10 \quad r^{(k)} = \frac{P(\underline{I}^{(k)} | \underline{Z})}{\sum_{l=1}^K P(\underline{I}^{(l)} | \underline{Z})} = \frac{P(\underline{Z}, \underline{I}^{(k)})}{\sum_{l=1}^K P(\underline{Z}, \underline{I}^{(l)})} = \frac{P(\underline{Z} | \underline{I}^{(k)}) P(\underline{I}^{(k)})}{\sum_{l=1}^K P(\underline{Z} | \underline{I}^{(l)}) P(\underline{I}^{(l)})} = \frac{e^{-\Lambda^{(k)}}}{\sum_{l=1}^K e^{-\Lambda^{(l)}}} \quad (3)$$

- where it is assumed that  $P(\underline{I}^{(k)})$  is the same for all  $k$ , due to the equiprobability of the transmitted data. In the conventional VA, all the information along the path is removed except the hard decisions for the survival path, but SOVA updates the *a posteriori* probability along the survival
- 15 path using the calculated reliability. That is,

$$P_{jm}^{(sp)} = \sum_{k=1}^K P_{jm}^{(k)} \cdot r^{(k)}, \quad j = n, n-1, \dots, n-\delta \quad \text{and} \quad m = 1, 2, \dots, M \quad (4)$$

where  $P_{jm}^{(sp)}$  is the *a posteriori* probability of the  $m^{\text{(th)}}$  channel symbol at time  $j$  for the survival path  $(sp)$ .

- In one embodiment, a reasonable choice for the soft output 6 may be
- 20 the conditional mean of the channel symbol along the (global) survival path, which is given by

$$\tilde{I}_j = \sum_{m=1}^M P_{jm}^{(sp)} \cdot I(m) \quad (5)$$

where  $I(m)$  is the channel symbol corresponding to the label  $m = 1, 2, \dots, M$ .

As an example, one could apply a Maximum-A-Posteriori (MAP) decoding algorithm. Some MAP algorithms are described in P. Robertson, E.

- 5 Villebrun and P. Hoeher, "A Comparison of Optimal and Sub-Optimal MAP Decoding Algorithms Operating in the Log Domain", Proceedings of ICC'95, Seattle, Washington, pp.1009-1013, June 1995. The SOVA decoder was considered since the HDTV system is not based on block processing and consequently, it is difficult to apply a bi-directional MAP decoder. However,
- 10 sliding window MAP decoding and unidirectional MAP decoding algorithms can be applied to this system since the basic algorithm is the same.

Referring also to Figure 4, a graph is presented that compares the Bit Error Rate (BER) to the Signal to Noise Ratio (SNR) for an HDTV receiver operating in the AWGN plus multipath channel. Figure 4 shows curves for a

- 15 hard output module 1 or a soft output module 1 when the original DFE 2 is in soft automatic decision mode: the original system without a module (marked by small diamonds, curve 9), the system with one module (marked by small squares), two modules (marked by stars, curves 12 and 15) and three modules (marked by small circles). In addition, Figure 4 shows curve 10,
- 20 representing the original system with the standard DFE in hard automatic switching mode. In this depiction, improved performance is indicated by obtaining the same error rate at a lower signal to noise ratio, or in other words, obtaining the same bit error rate when processing a weaker signal.

The multipath channel that is the basis of the curves in Figure 4 consists of a  
 25 single three decibel (dB), three microsecond ghost, which can be characterized as a relatively strong ghost signal. The depicted performance is measured at the output 11 of the trellis decoder 3. The curve 10 depicts the performance at the output 11 of the trellis decoder 3, when module 1 is not present in Figure 3 and the original DFE system depicted in Figure 1 is

operating in the automatic (hard) switching mode. In the (hard) automatic switching mode, the equalizer 2 is operating in the blind mode prior to convergence and switches to the hard, decision directed mode after convergence is detected. If convergence is lost, the equalizer 2 switches 5 back to the blind operating mode.

The curve 9 is similar to curve 10 but depicts the performance of the first equalizer 2 in the soft automatic switching mode. In the soft automatic switching mode, the hard, decision directed mode is replaced by the soft decision directed mode, but is otherwise identical to the (hard) automatic 10 switching mode for the purposes of switching based on the convergence status. When equalizer 2 is operating in the soft decision directed mode, the input to the FBF filter in Figure 1 is the output of the equalizer 2 as opposed to the slicer output produced when operating in the (hard) automatic switching mode.

All of the comparisons that are to be made concerning the curves depicted in Figure 4 are based on the Threshold of Visibility (TOV) point 20 for an ATSC HDTV system, which requires a bit error rate of approximately 0.002 at the trellis decoder output 11. The performance of curve 9 at its TOV point 14 results in an SNR requirement for input signal 21 of approximately 15 18.7 dB. Curve 12 represents the BER vs. SNR curve for two (and three) concatenated stages of the hard output embodiment of module 1, and at its TOV point 13 the input signal 21 is seen to have an SNR requirement of 20 approximately 18.2 dB, representing a 0.5 dB gain in performance. When utilizing two stages of the soft output embodiment of module 1, represented 25 by curve 15, the SNR requirement at the TOV point 16 is approximately 17.6 dB, representing an approximately 1.1 dB improvement over the original system operating in the soft automatic switching mode as depicted by curve 9. The two stage implementation of the soft output embodiment of module 1 has approximately 0.6 dB more gain than the corresponding hard output 30 embodiment (17.6 dB vs. 18.2 dB, respectively), which comes at the expense

of the increased complexity associated with the soft output (SOVA) algorithm. Finally, when the original system of the standard DFE of Figure 1 depicted by curve 10 is compared at its TOV point 22 with the soft output embodiment of module 1, the performance improvement of the present invention is  
5 approximately 1.9 dB (17.6 dB at point 16 vs. 19.5 dB at point 22).

The concatenated architecture of the present invention can also be associated with the original system shown in Figure 1, in which the equivalent of first equalizer 2 is the standard DFE operating in the (hard) automatic switching mode. Although the results shown in Figure 4 show improved  
10 performance when using the soft automatic switching mode for the first equalizer 2, this may not necessarily be the case for all channels. Figure 5 depicts the case of the BER versus SNR performance curves for the multipath channel consisting of a single three decibel, three microsecond ghost, which again is a relatively strong ghost signal. The performance depicted is  
15 measured at the trellis decoder output 11. Figure 5 shows curves for a soft output module 1 when the original DFE 2 is either in hard automatic switching mode or soft automatic decision mode: the original systems without a module (curves 10 and 9), the systems with one output soft module (represented by small squares), two soft output modules (represented by stars, curves 23 and  
20 24) and three soft output modules (represented by small circles). The curves 9 and 10 representing the original system of Figure 1 in the soft and (hard) automatic modes, respectively, remain unchanged from Figure 4. The remaining curves represent the use of the soft output embodiment of module 1 with first equalizer 2 in either the (hard) automatic switching mode or the  
25 soft automatic switching mode. The curve 23 represents the performance of the first equalizer 2 operating in the (hard) automatic switching mode when using two stages of module 1, and the TOV point 25 shows a SNR requirement at equalizer input 21 of approximately 18.2 dB. The curve 24 is for the first equalizer 2 operating in the soft automatic switching mode  
30 followed by two stages of module 1. The TOV point 26 shows an SNR requirement of 17.6 dB, or an approximately 0.6 dB improvement when

compared to the (hard) automatic switching mode depicted by curve 23. For the higher SNR regions depicted by, for example, point 27 (greater than 18.6 dB), the curve 9 for the original system and soft automatic switching mode and the curve 28 for the (hard) automatic switching mode plus one soft output module 1 are seen to merge into approximately equivalent performance .

Although the concatenated equalizer/trellis decoder architecture of the present invention is designed primarily for use with the ATSC HDTV equalizer, the same principle can be usefully applied to any general equalizer arrangement that employs a DFE in a system where the equalizer is followed by a trellis or convolutional decoder. For such a system the error propagation into the DFE filter originated by linear distortion, noise and the presence of the slicer in the decision directed (dd) mode results in noise bursts at the equalizer output which will tend to impair decoder performance.